**BPDC, Dubai - First Semester, 2022-2023**

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| **Course No: CS F342** |  | **Course Title: Computer Architecture** |

Q1.

For a 32KB direct mapped cache with 128 byte cache block, give the address of the starting byte of the first word in the block that contains the following address. 0x A23847EF

Block size is 128 byte = 27 .

2index = cache size / (block size x associativity) = 215 / (27 x 1) = 28 . 8 bits used for index

Least significant 7 bits used as block offset.

Change least significant 7 bits (0x A23847**EF**) to zero to represent the starting byte of the first word in the block. EF -> 1110 1111 🡺 1000 0000

Answer: 0x A23847**80**

Q2. A cache has 256 KB capacity, 1B word, 128 byte block size and 4-way set associative. The system is using 32 bit address. Given the following addresses, which set of cache will be searched and specify which byte of the selected cache block will be forwarded if it is a hit in cache?

0x ABC89987

Block size is 128 byte = 27 .

2index = cache size / (block size x associativity) = 218 / (27 x 22) = 29 . 9 bits used for index.

|  |  |  |
| --- | --- | --- |
| Tag | Index | Block offset |
| 16 | 9 | 7 |

Least significant 7 bits used to represent the byte of the selected cache block.

(0x ABC89987 = = > 1010 1011 1100 1000 1001 1001 1**000 0111**  = = > 7

Next 9 bits used to represent the which set of the selected cache block.

(0x ABC89987 = = > 1010 1011 1100 1000 **1001 1001 1**000 0111 = = > 307

Q3. It takes 2.5ns to access a tag array value and 4ns to access a data array, 1ns to perform hit/miss comparison and 1ns to return the selected data to processor. a) What is the cache hit latency of the system? b) What would be the hit latency of the system if both tag and data array access take 2.5ns and hit/miss comparison take 1ns?

Search in tag array and data array will be done simultaneously.

1. Tag array will take 2.5 + 1 = 3.5ns.

Max{ 3.5, 4} = > 4 + 1ns(to return the selected data to processor) => 5ns

1. Tag array will take 2.5 + 1 = 3.5ns.

Max{ 3.5, 2.5} = > 3.5 + 1ns(to return the selected data to processor) => 4.5ns

Q4. A cache has hit rate = 95%, 128 byte block, cache hit latency = 5ns. Main memory takes 100ns to return first word (32bits) of a block and 10ns for each subsequent word. What is the miss latency of the cache? What is AMAT?

#words = 128byte/4byte = 32words

100ns to return first word (32bits) of a block and 10ns for each subsequent word.

= 100 + 31x10 = 410

AMAT = Hit Time + Miss Rate x Miss Penaly

= 5 + 0.05 x 410